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Description

SEMICONDUCTOR PACKAGE AND METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a semiconductor package, and more specifically, to a ball grid array (BGA) semiconductor package having a plurality of solder balls arranged in a single line.

[0003] 2. Description of the Prior Art

[0004] Integrated circuit (IC) packages generally include PTH (pin through hole) types and SMT (surface mount technology) types. Since the SMT type package has advantages of a large number of I/O pins, high heat dissipation and a small size, the SMT type package has played an important role in the IC package industry. Additionally, the SMT type package adopts solder balls instead of leads, and the SMT

type package usually includes a BGA package and a chip scale package (CSP), which can be regarded as an ultra small BGA package.

[0005] Please refer to Fig.1 and Fig.2. Fig.1 is a bottom view of a prior art semiconductor package. Fig.2 is a cross-sectional view along line 2-2' of Fig.1. As shown in Fig.1 and Fig.2, a semiconductor package 10 includes a substrate 12 having an upper surface 12a and a lower surface 12b, a chip 14 positioned on the upper surface 12a of the substrate 12, a plurality of bonding pads 18 positioned on the lower surface 12b of the substrate 12, and a plurality of solder balls 16 respectively positioned on the bonding pads 18. The chip 14 is an image sensor chip, such as a charge coupled device (CCD) or a CMOS image sensor device, and the chip 14 can be connected to the substrate 12 by using a wiring bonding method or a flip-chip method. Additionally, the semiconductor package 10 is electrically connected to a printed circuit board (PCB) 20 for forming a BGA package. Generally, the printed circuit board 20 includes a plurality of bonding pads (not shown), each of which is positioned between the printed circuit board 20 and each of the solder balls 16.

[0006] Due to the progress of the semiconductor technology,

electronic devices in the chip 14 are made smaller and smaller so that the chip 14 is generally shrinking in size. Accordingly, a width W and a length L of the chip 14 are gradually reduced, such that dimensions of each solder ball 16 and a distance between two adjacent solder balls 16 have to be decreased. However, due to process limitations, the dimensions of each solder ball 16 and the distance between two adjacent solder balls 16 cannot be reduced without limitation. That is, dimensions of the chip 14 can be reduced until the lower surface 12b of the substrate 14 accommodates only a single row of solder balls 16. Nevertheless, as shown in Fig.3, when the semiconductor package 10 is electrically connected to the printed circuit board 20 via the solder balls 16 arranged in a single line, the semiconductor package 10 on the printed circuit board 20 may incline to one side easily, which changes an incident angle between incident light and the image senor chip 14, thereby degrading sensing accuracy of the image senor chip 14.

SUMMARY OF INVENTION

[0007] It is therefore a primary objective of the claimed invention to provide a semiconductor package for solving the above-mentioned problem.

[0008] According to the claimed invention, a semiconductor package is provided. The semiconductor package positioned on a first substrate includes a second substrate having a first surface and a second surface, a chip positioned on the first surface of the second substrate, a plurality of first bonding balls positioned on the second surface of the second substrate and arranged in a line along a first direction for connecting the second substrate to the first substrate, andat least a dummy bonding bar positioned on the second surface of the second substrate for connecting the second substrate to the first substrate and preventing the semiconductor package from inclining to one side.

[0009] It is an advantage over the prior art that the claimed invention provides at least one dummy bonding bar of the second surface of the second substrate, so that the semiconductor package can be effectively prevented from inclining to one side.

[0010] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the multiple figures and drawings.

Brief Description of Drawings

[0011] Fig.1 is a bottom view of a prior art semiconductor package.

[0012] Fig.2 is a cross-sectional view along line 2-2' of Fig.1.

[0013] Fig.3 is a cross-sectional view of a prior art semiconductor package having solder balls arranged in a single line.

[0014] Fig.4 is a bottom view of a semiconductor package according to the first embodiment of the present invention.

[0015] Fig.5 is a cross-sectional view along line 5-5' of Fig.4.

[0016] Fig.6 is a cross-sectional view along line 6-6' of Fig.4.

[0017] Fig.7 is a bottom view of a semiconductor package according to the second embodiment of the present invention.

[0018] Fig.8 to Fig.11 are schematic diagrams illustrating a method for manufacturing a semiconductor package according to the present invention.

[0019] Fig.12 is a bottom view of a semiconductor package according to the third embodiment of the present invention.

Detailed Description

[0020] Please refer to Fig.4 to Fig.6. Fig.4 is a bottom view of a semiconductor package according to the first embodiment

of the present invention. Fig.5 is a cross-sectional view along line 5-5' of Fig.4.Fig.6 is a cross-sectional view along line 6-6' of Fig.4. As shown in Fig.4 and Fig.5, a semiconductor package 30 includes a substrate 32 having an upper surface 32a and a lower surface 32b, a chip 34 positioned on the upper surface 32a of the substrate 32, a plurality of bonding pads 38 positioned on the lower surface 32b of the substrate 32, and a plurality of bonding balls 36 respectively positioned on the bonding pads 38. The chip 34 is an image senor chip, such as a CCD or a CMOS image sensor chip, and the chip 34 can be connected to the substrate 12 by using a wiring bonding method or a flip-chip method. Additionally, the chip 34 has a rectangular shape, the bonding balls 36 are arranged in a line along a long side of the chip 34, and a length of a short side of the chip 34 is less than 1000 μm. The substrate 32 can be a build-up printed circuit board, a co-fired ceramic substrate, a thin-film deposited substrate or a glass substrate.

[0021] As shown in Fig.5 and Fig.6, the semiconductor package 30 further includes a dummy bonding pad 44 positioned on the lower surface 32b of the substrate 32, and a dummy bonding bar 42 positioned on the dummy bond-

ing pad 44 and having a planar surface 42a. Additionally, a height h_2 of the dummy bonding bar 42 is approximately equal to a height h_1 of each bonding ball 36. Furthermore, the semiconductor package 30 is connected to a printed circuit board 40 via the bonding balls 36 and the dummy bonding bar 42 for forming a BGA package. The printed circuit board 40 usually includes a plurality of bonding pads (not shown), each of which is positioned between the printed circuit board 40 and each of the dummy bonding bar 42 and the bonding balls 36. The dummy bonding bar 42 and the bonding balls 36 are composed of tin (Sn).

[0022] Since the dummy bonding bar 42 has the planar surface 42a, there is a surface contact between the dummy bonding bar 42 and the printed circuit board 40 when the surface 42a of the dummy bonding bar 42 is connected to the printed circuit board 40. Further, because the longest side of the dummy bonding bar 42 is approximately perpendicular to the long side of the chip 34, the semiconductor package 30 can be balanced on the printed circuit board 40, thereby preventing the semiconductor package 30 from inclining to one side. Additionally, a shape, a position, and an amount of the dummy bonding bar 42 are

not limited to those shown in Fig.3 and can be changed according to process requirements. Therefore, please refer to Fig.7, which is a bottom view of a semiconductor package according to the second embodiment of the present invention. As shown in Fig.7, a semiconductor package 30 includes a substrate 32, a plurality of bonding balls 36 positioned on the substrate 32, and two dummy bonding bars 42 positioned on the substrate 32 and among the bonding balls 36.

[0023] Please refer to Fig.8 to Fig.11. Fig.8 to Fig.11 are schematic diagrams illustrating a method for manufacturing a semiconductor package according to the present invention. Additionally, Fig.8 to Fig.11 are cross-sectional views along line 8-8' of Fig.4. As shown in Fig.8, a substrate 32 is firstly provided. Then, a plurality of bonding pads 38 and a dummy bonding pad 44 are formed on the substrate 32 by using thin-film deposition processes, photolithographic processes and etching processes. Thereafter, a stencil plate 46 is provided and the stencil plate 46 has a plurality of openings 46a respectively corresponding to the bonding pads 38 and the dummy bonding pad 44. As shown in Fig.9, the stencil plate 46 is put on the substrate 32 such that the bonding pads 38

and the dummy bonding pad 44 are exposed. After that, solder paste 48 is coated in the openings 46a of the stencil plate 46, and then, the stencil plate 46 is separated from the substrate 32. As shown in Fig.10, a thermal treatment process is performed on the substrate 32 for melting the solder paste 48, thus forming the bonding balls 36 and the dummy bonding bar 42. Additionally, the solder paste 48 can be a tin (Sn) based metal containing lead (Pb) or a tin based metal that contains no lead, and the solder paste 48 has a melting point between 180°C and 235°C . Furthermore, the bonding pads 38 and the dummy bonding pad 44 are composed of a tin based metal, which contains no lead and has a melting point between 180°C and 235°C . In another embodiment of the present invention, the stencil plate 46 can be replaced with a screen sheet.

[0024] Finally, the chip 34 is connected to the substrate 32 by using a wiring bonding method or a flip-chip method, as shown in Fig.11. In addition, the bonding balls 36 and the dummy bonding bar 42 can be made by using an electroplating method, an electroless plating method, an evaporation method or a laser ball shooter.

[0025] In addition, the structure of the semiconductor package

30 is not limited to those shown in Figs.4-6, and the following description will introduce other embodiments of the present invention. Please refer to Fig.12. Fig.12 is a bottom view of a semiconductor package according to the third embodiment of the present invention. For convenience of explanation, the sameelements of Figs.4-6 and Fig.12 are indicated by the same symbols. As shown in Fig.12, a semiconductor package 30 includes a substrate 32, a plurality of bonding balls 36a and bonding balls 36b positioned on the substrate 32, and at least one dummy bonding bar 42 positioned on the substrate 32. Particularly, the bonding balls 36a are interlaced with the bonding balls 36b.

[0026] In comparison with the prior art, the present invention provides at least one dummy bonding bar 42 on the lower surface 32b of the substrate 32. Since the dummy bonding bar 42 has the planar surface 42a, there is a surface contact between the dummy bonding bar 42 and the printed circuit board 40 when the surface 42a of the dummy bonding bar 42 is connected to the printed circuit board 40. Further, because the longest side of the dummy bonding bar 42 is approximately perpendicular to the long side of the chip 34, the semiconductor package 30

can be balanced on the printed circuit board 40, thereby effectively preventing the semiconductor package 30 from inclining to one side.

[0027] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bound of the appended claims.